REMARKS

SUPPLEMENTAL IDS

A supplemental IDS is filed contemporaneously herewith. The Hashimoto reference was cited in an office action for serial No. 09/811,844. That reference discloses resistive elements on opposite surfaces of the substrate. However, Hashimoto is directed towards a chip resistor with a high accuracy correction of resistance value (Abstract) and not to providing a surge current chip resistor.

ISSUES UNDER 35 U.S.C. § 102

The examiner has rejected claims 1-3 and 5-8 under 35 U.S.C. § 102 (B) as being anticipated by U.S. Patent 4,901,052 to Chapel, Jr. et al. As Chapel, Jr. et al. does not disclose each and every limitation of the Applicants' claimed invention, the Applicants respectfully traverse.

Claim 1 requires "separate and spaced first and second resistive layers on the first and second surfaces, respectively, electrically connected in parallel to each other." This limitation is simply not disclosed by Chapel, Jr. et al. In Chapel there simply are not the first and second surfaces, each with a resistive layer. Also note that the first and second surfaces are "opposite parallel symmetrical first and second surfaces." These limitations of claim 1 are not disclosed in Chapel, Jr. et al. The Examiner previously indicated that Figure 5 discloses these limitations (Office Action, numbered paragraph 2). This is simply incorrect. First, the Applicant notes that Figures 5a and 5b show a plan view of a resistor network (column 7, lines 51-54). Thus, it is clear from the figures of Chapel Jr, et al. that the elements of the resistive network are located on the **same** surface.

Thus, Chapel, Jr. et al. simply does not disclose this limitation and physical structure of the claimed invention. Thus this rejection should be withdrawn on that basis.

In addition, there are other bases for withdrawing this rejection. For example claim 1 requires "the first and second surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof." The Applicant directs the Examiners attention to the last paragraph of page 7 of the specification in which the Applicant explains:

> "Another type of resistor failure involves solder joint fatigue. It may be shown that prior art chip resistor loaded by pulse is characterized by monotone decreasing temperature distribution in direction from resistive layer to the opposite free surface of the substrate. This temperature distribution results in monotone decreasing of thermal expansion of the substrate in the same direction. It becomes apparent in the substrate bending. The bending creates mechanical stress in the solder joints between the chip and printed circuit board. Multiple application of the pulses may result in solder joint fatigue (cracking)."

Thus, Chapel, Jr. et al does not provide the advantage of "a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof." Thus, for this additional reason, this rejection should be withdrawn.

As claims 2-3 and 5-8 depend from claim 1, the Applicant submits that these rejections should also now be withdrawn.

ISSUES UNDER 35 U.S.C. § 103

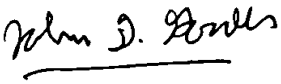
Claim 4 has been rejected under 35 U.S.C. § 103(a) being inpatentable over U.S. Patent 4,901,052 to Chapel, Jr. et al in view of U.S. Patent 4,064,477 to Thompson. In particular, the

Examiner indicates that Thompson discloses a foil resistive layer (office action, page 3, numbered paragraph 4). The Applicant agrees that Thompson discloses a foil resistive layer. Nevertheless, neither Thompson nor Chapel alone or in combination disclose each and every limitation of claim 1. Claim 4 depends from claim 1, and Thompson does not disclose "separate and spaced first and second resistive layers on the first and second surfaces, respectively, electrically connected in parallel to each other; and the first and second surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof." Therefore, this rejection should be withdrawn.

No fees or extensions of time are believed to be due in connection with this amendment; however, consider this a request for any extension inadvertently omitted, and charge any additional fees to Deposit Account No. 26-0084.

Reconsideration and allowance is respectfully requested.

Respectfully submitted,



JOHN D. GOODHUE Reg. No. 47,603
McKEE, VOORHEES & SEASE, P.L.C.
801 Grand Avenue, Suite 3200
Des Moines, Iowa 50309-2721
Phone No. (515) 288-3667
Fax No. (515) 288-1338
CUSTOMER NO: 22885

Attorneys of Record

mlw